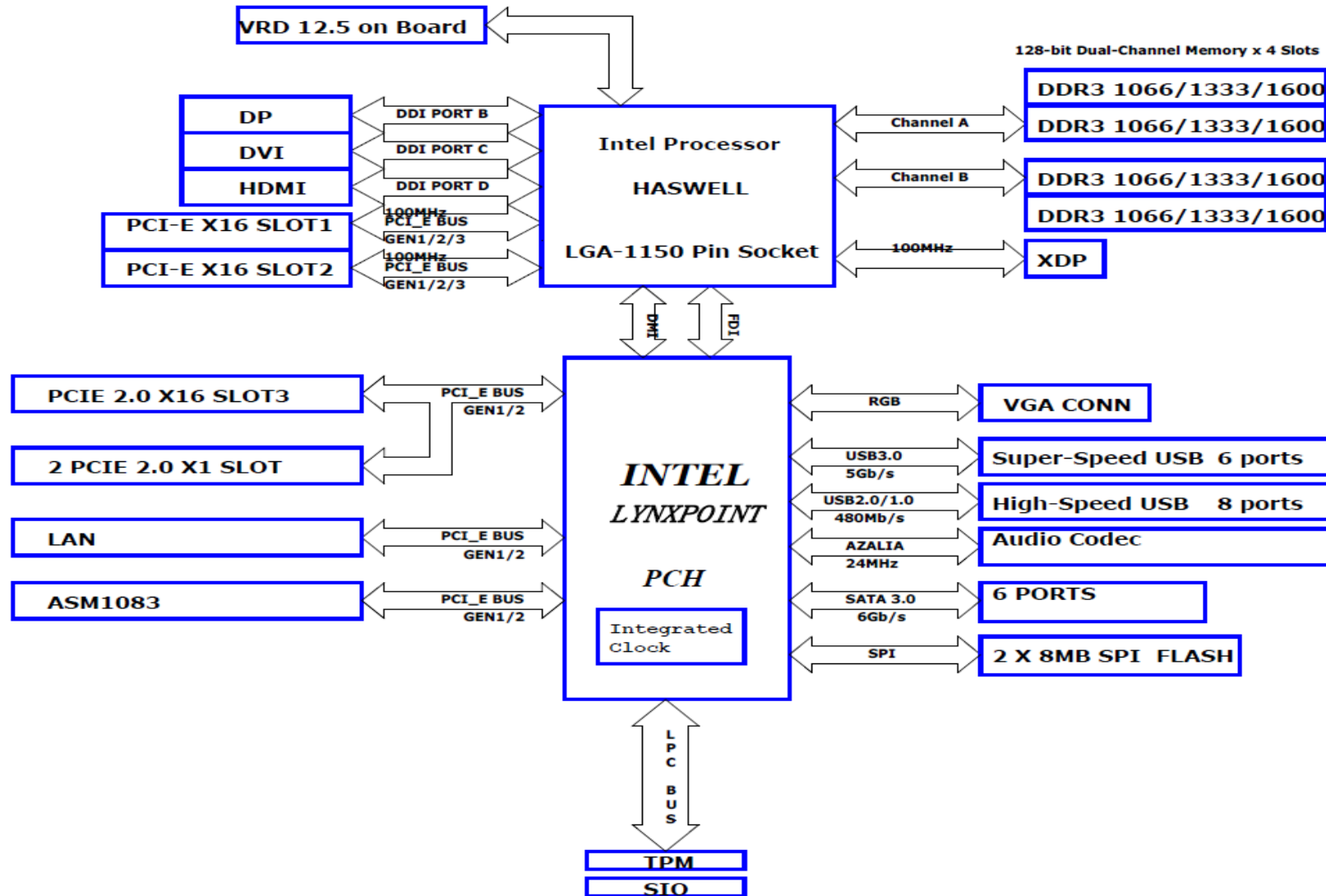


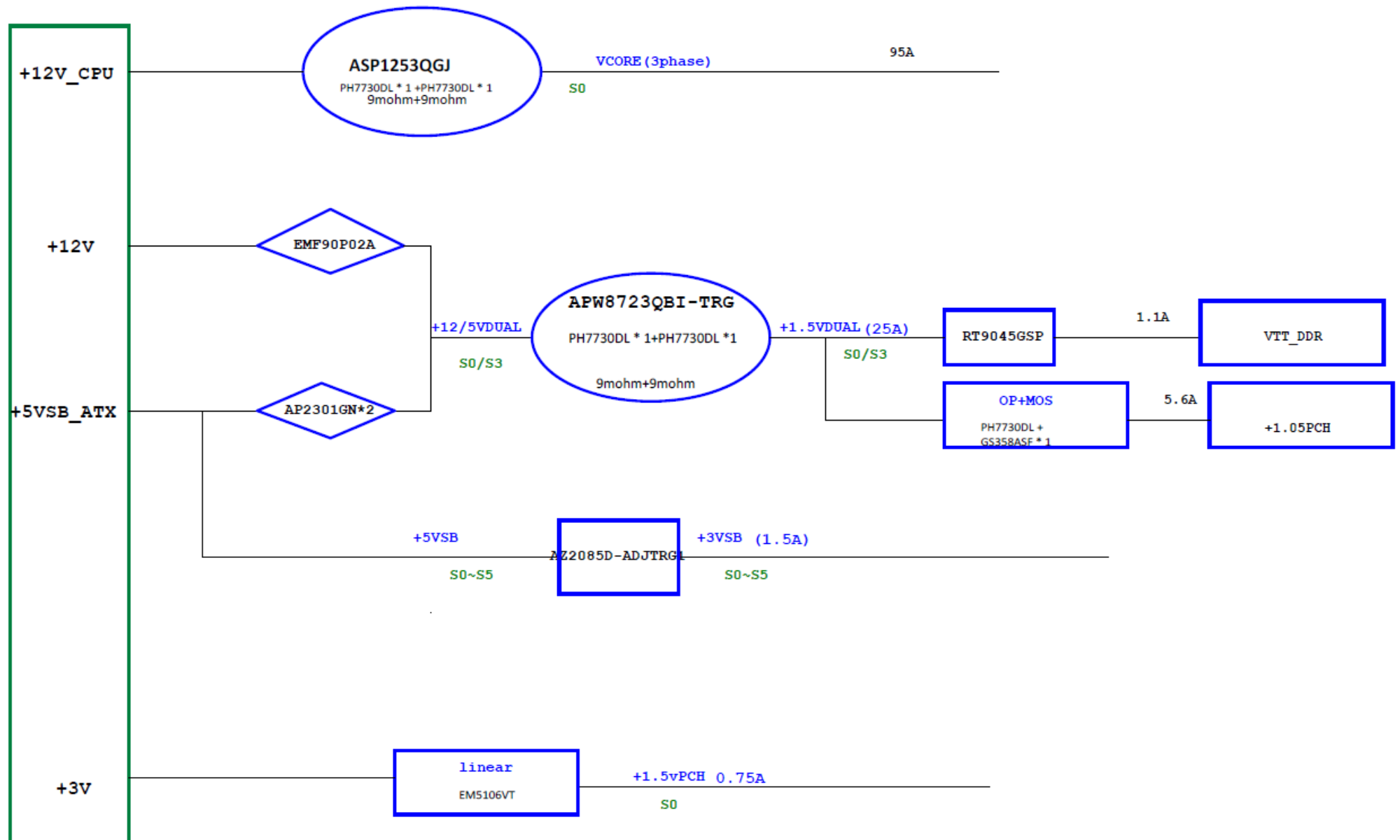
H81M-C Repair Guide

07/162013
Leilei52_Chen
CSC-GRMA

BLOCK DIAGRAM



POWER FLOW



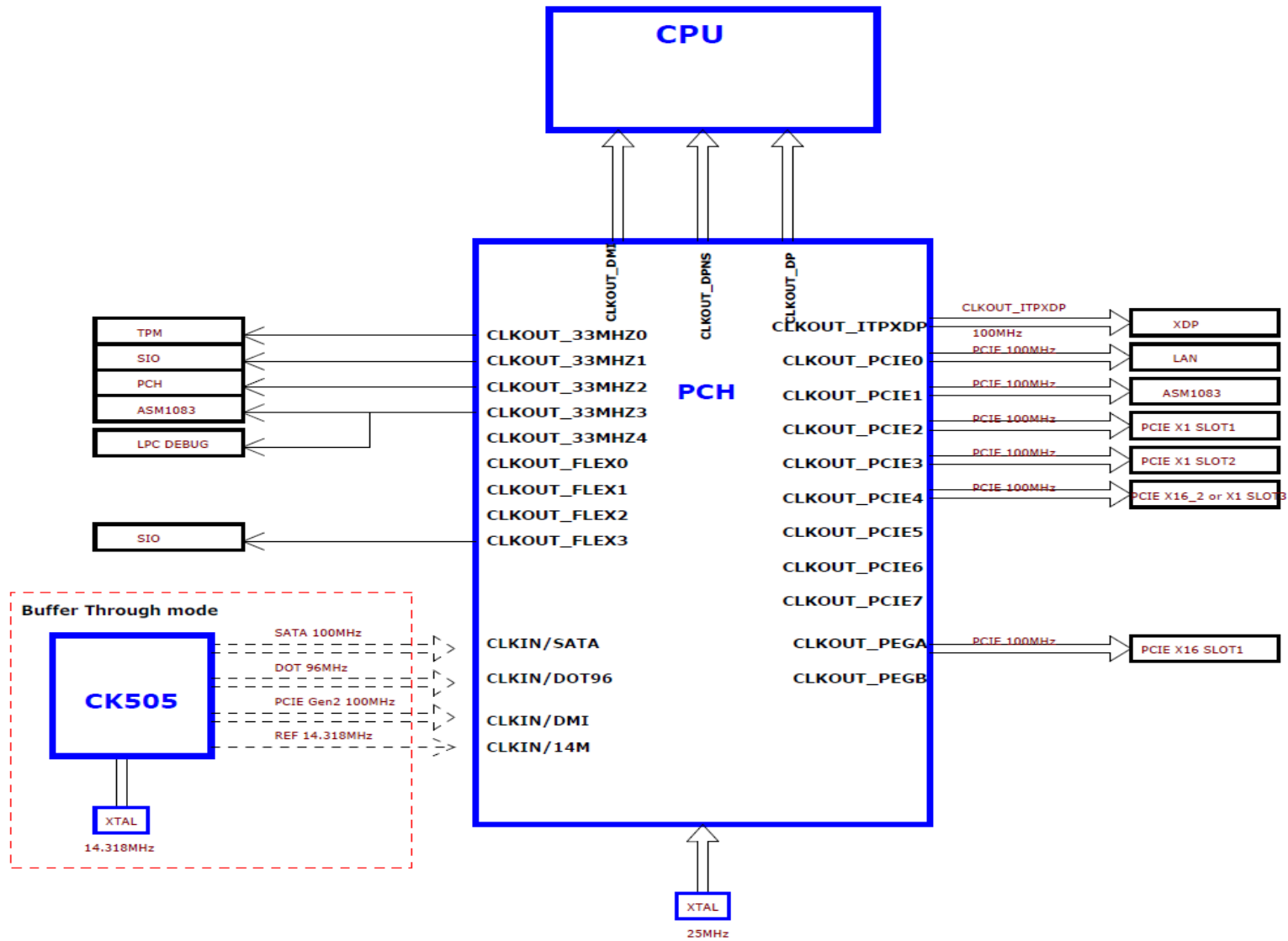
Vinafix.com

```

1 PSON# is inverted by SLP_S3#,
2 but gated and delayed by
3 PWRBTN#
4
5 PWROK will assert when +3V arrives
6 at +2.1V then delay 300ms-500ms
7 and gated by ATXPGD
8
9 If support AMT, SLP_A#
10 could already be high
11 before sequence begins.
12 If not support AMT, SLP_A#
13 will come with SLP_S3
14
15 SLP_S4# controls +1.5VDual and
16 +VTTDDR
17
18 Come with 1.5VDUAL
19
20 Come with +3V,+12V and gated
21 by SLP_S3#
22
23 CPUFWGRD= After PWROK
24
25 PLTRST# = PCH PWROK "AND" PCH
26 SYS_PWROK
27
28 PLTRST_PROC#=PLTRST#,
29 voltage=1V, directly connect
30 to CPU

```

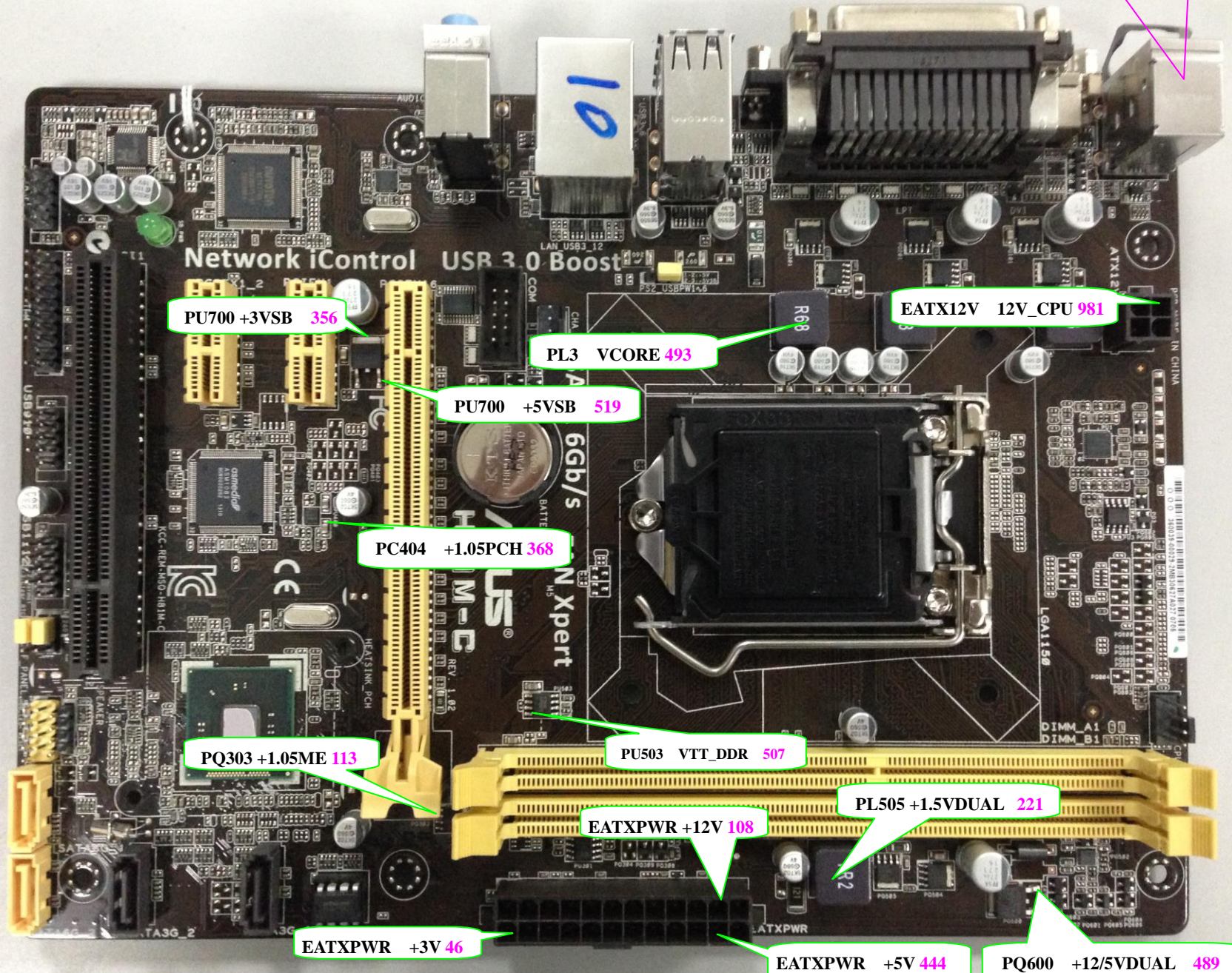
Frequency Flow



Voltage Measure Point

Pink number is Diode resistance to GND(without any part on MB)multimeter type DH-1240

multi meter "VΩmA" port touch here



Signal Measure Point

